RICHARD DAYSTROM

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EXPERIENCE

Senior Hardware Engineer, *Apple*, Ithaca, NY — Aug 2024 - Present

- Help design and integrate new hardware features for Apple Silicon SoCs used in Mac laptops and desktops.
- Work with chip architects and verification teams to define module requirements and evaluate new hardware ideas.
- Write, simulate, and refine RTL (Verilog/SystemVerilog) for on-chip components such as bus interfaces, memory paths, and control logic.
- Review timing reports and support timing closure to ensure the design meets clock, power, and area targets.
- Support early silicon bring-up by helping debug failures, validate hardware behavior, and refine test plans.

Principal Hardware Engineer, *NVIDIA*, Ithaca, NY — Nov 2018 - Jul 2024

- Designed digital hardware for high-performance GPU memory subsystems, including memory controllers, cache structures, and on-chip interconnects.
- Led small hardware and verification teams through design, simulation, reviews, and sign-off for multiple GPU IP blocks.
- Improved memory performance by refining address pipelines, arbitration logic, and data-flow scheduling.
- Ensured designs met DDR5, GDDR6, and PCIe electrical and timing requirements.
- Supported FPGA prototyping and pre-silicon testing to verify functionality before tape-out.

Hardware Engineer, *Tesla*, Ithaca, NY — Sep 2016 - Oct 2018

- Led firmware development for vehicle infotainment and driver-assistance systems across multiple Tesla models.
- Built real-time embedded software for ARM processors running Linux and QNX, improving system response times.
- Supported safety audits and reviews, ensuring all software met functional-safety requirements.
- Guided teams during fault analysis and helped implement safer, more stable system behavior.

Hardware Design Engineer I, *Intel*, Ithaca, NY — May 2015 - Sep 2016

- Designed digital logic modules in Verilog for signal processing and communication subsystems.
- Created FPGA-based prototypes to test new hardware features before ASIC development.
- Ran timing analysis, simulations, and hardware tests to verify design behavior.
- Worked with senior engineers to review schematics, block diagrams, and system layouts.

Hardware Engineering Intern, *Intel*, Ithaca, NY — May 2014 - May 2015

- Assisted with FPGA timing analysis and logic optimization for internal test platforms.
- Wrote small Verilog modules and testbenches under guidance from senior designers.
- Helped run simulation tests and document results for design reviews.

EDUCATION

BSCE, *Cornell University*, College of Engineering — May 2015

SKILLS

- **Stack:** C, C++, Python, Assembly, FreeRTOS, QNX, VxWorks, Bootloaders, AUTOSAR
- **Hardware:** Verilog, VHDL, SystemVerilog, SystemC, Chisel, High-Level Synthesis, RTL Design