MAJOR BOOTHROYD

majorboothroyd@gmail.com | (481) 516-2342 | Cambridge, MA | Portfolio/GitHub/LinkedIn

EDUCATION

Massachusetts Institute of Technology, School of Engineering — Expected: May 2026
B.S. Computer Engineering — GPA: 3.8

EXPERIENCE

Software Engineering Intern, *AMD*, Cambridge, MA — May 2024 - Present

- Built an automated test system using Python and Jenkins that sped up graphics driver testing by 6 hours each release.
- Worked with hardware and firmware teams to fix BIOS boot issues, resolving almost all high-priority bugs the same day.
- Wrote clear documentation for software tools and APIs, making onboarding faster and reducing repeated questions from the team.

Undergraduate Research Assistant, *Computer Architecture Lab*, Cambridge, MA — Jan 2024 - Present

- Designed a RISC-V processor core in Verilog and deployed it on an FPGA, improving speed and reducing delays in the processor pipeline.
- Tested performance using standard benchmarks, reaching efficiency close to a Cortex-M4 processor.
- Reviewed timing and synthesis reports to find and fix slow points in the design, presenting results at a research forum.

PROJECTS & LEADERSHIP

Vice President, IEEE Student Chapter — May 2023 – May 2024

- Organized hands-on workshops on PCB design, FPGA programming, and embedded Linux for more than 80 students each semester.
- Led a team of 12 students in a hardware competition, building a smart-home system with ESP32 devices and earning second place out of 25 teams.

Real-Time Operating System (RTOS) Kernel, Embedded Systems Course Project — Jan 2024 - Apr 2024

- Built core RTOS features such as semaphores, mutexes, and message queues to ensure safe communication between tasks.
- Created a memory manager that improved RAM use and prevented fragmentation.
- Wrote device drivers for UART, SPI, and I2C and built a real-time sensor logging demo.

Machine Learning Accelerator Hardware Design, Digital Logic Design Project — Sep 2023 - Dec 2023

- Designed a simple neural-network hardware accelerator in Verilog using a systolic array for fast matrix multiplication.
- Improved throughput and reduced latency compared to running the same model on a standard ARM processor.

SKILLS

- **Stack:** C, C++, Python, Java, Verilog/VHDL, SystemVerilog, Assembly, MATLAB, SQL
- **Hardware:** ARM Cortex-M Series, RISC-V Architecture, Raspberry Pi, Arduino, ESP32, STM32, FPGA Development, PCB Design, Oscilloscope, Logic Analyzer